CSCI 2570 Introduction to Nanocomputing

Introduction to NW Decoders

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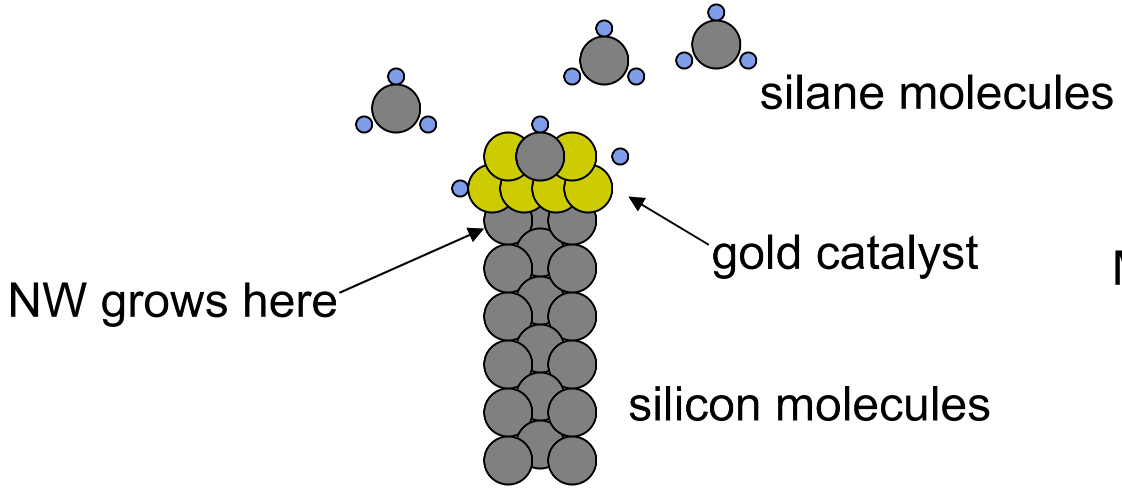
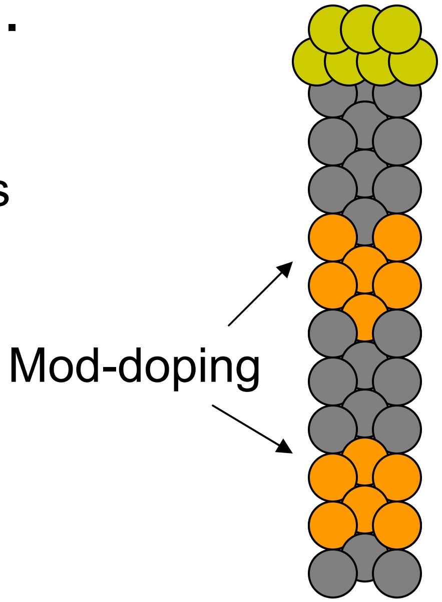
Lecture Outline

- Growing nanowires (NWs)
- Crossbar-based computing
- Types of NW decoders
- Resistive model of decoders
- Addressing strategies for decoders
- Area efficiency of decoders.

Encoded Nanowires Grown by Chemical Vapor Deposition

- Semiconducting NWs grown from seed catalysts; their diameters controlled by seed.

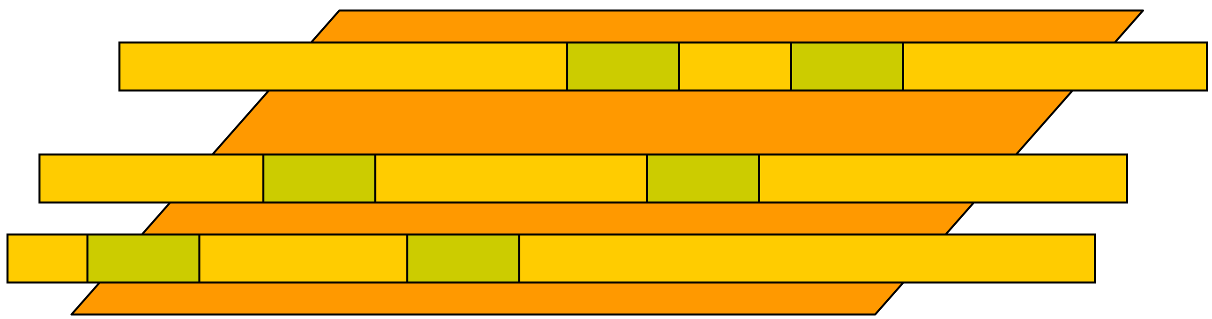




- **Modulation Doping**: dopants added to gas as NWs grow; doped sections have lithographic length.

Fluidic Assembly of Differentiated NWs

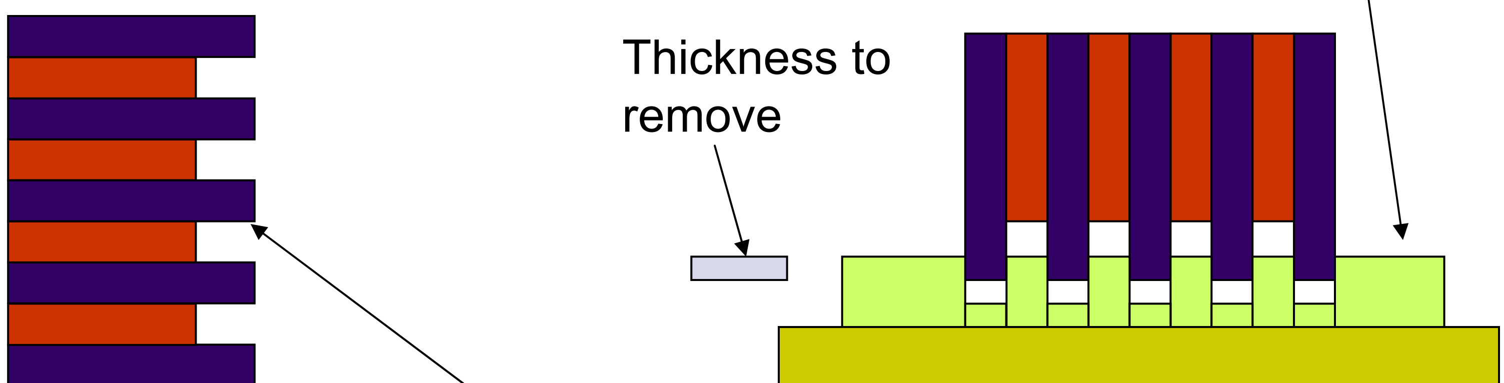
- Random sample of coded NWs is floated on a liquid, deposited on chip, and dried.



- NWs self-assemble into parallel locations.
- Process repeated at right angles – crossbar.

Uniform NWs via Nanolithography

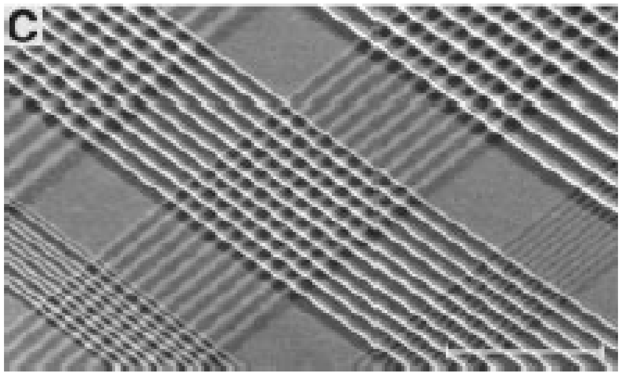
- Impress sawtooth pattern on soft polymer.
- Remove thin layer of polymer
- Deposit NWs in gaps as per lithography



Alternating layers of two materials. Etch away one of them to form sawtooth pattern.

Uniform NWs

- NWs produced by SNAP process

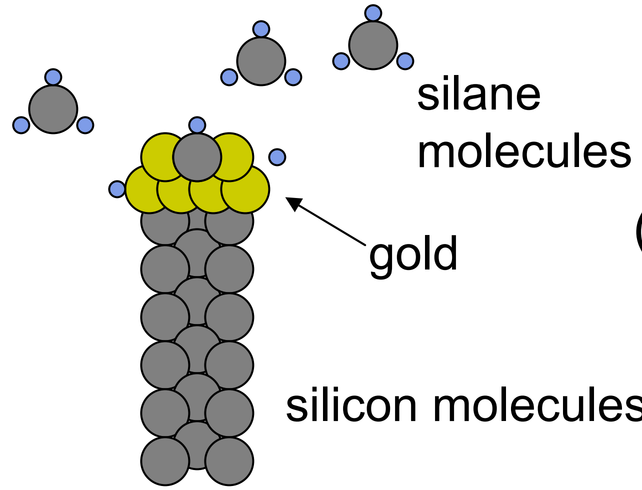


@ Science, Melosh et al., vol 300, April 2003.

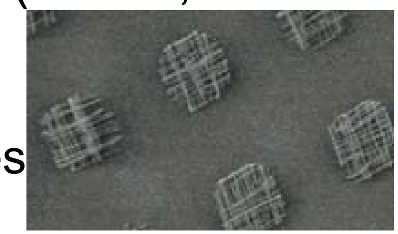
- Use nanolithography to deposit metal on substrate containing S_i on S_iO_2 on S_i. Etch away S_i between wires, remove wires to reveal S_i wires.

Growing Nanowires to Make Crossbars

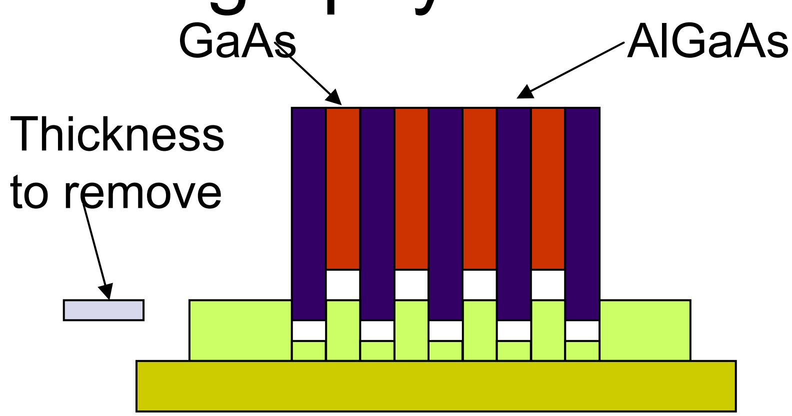
- Chemical vapor deposition (CVD).
- Fluidic assembly.



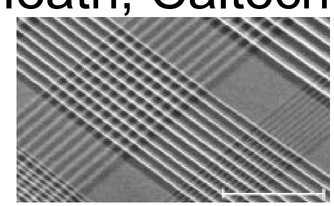
CVD NWs
(Lieber, Harvard)



- Nanoimprint lithography



SNAP NWs
(Heath, Caltech)

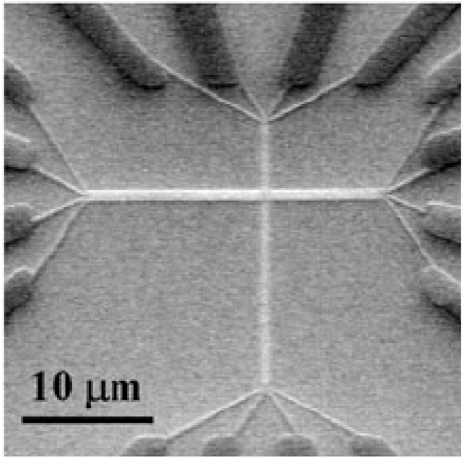


Controlling NW Crosspoints

- What happens if each NW must be connected to one MW?
  - A lot of area is wasted!

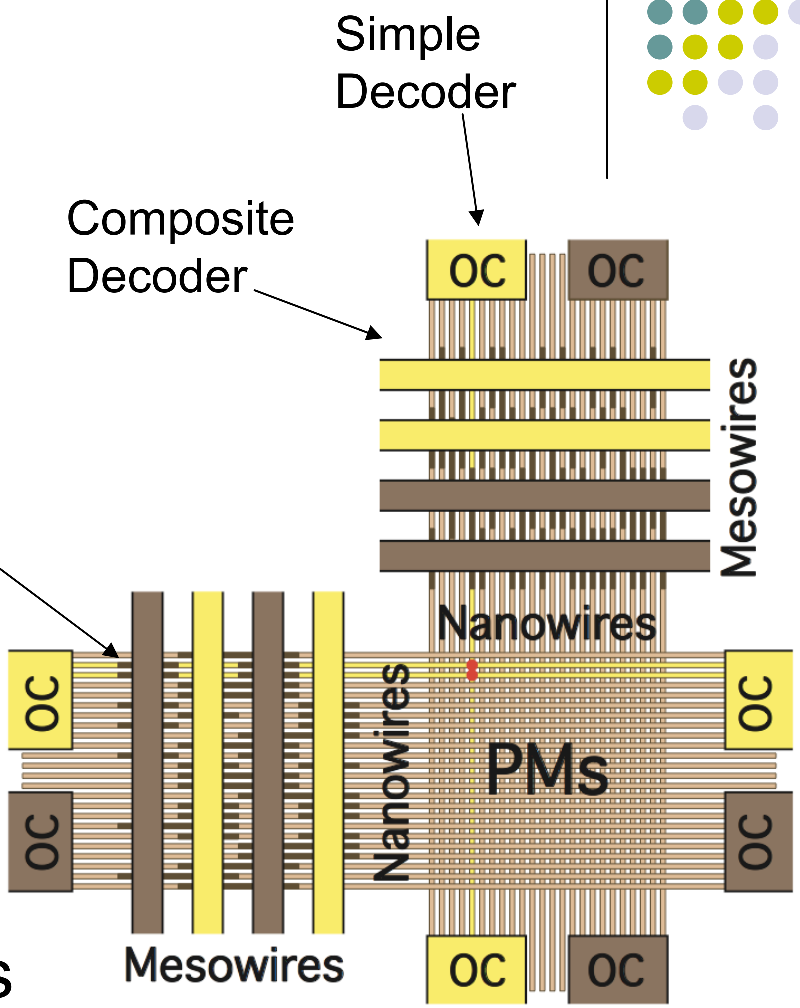
- Goal: control many NWs with few MWs.

Controlling NWs (Heath, Caltech)



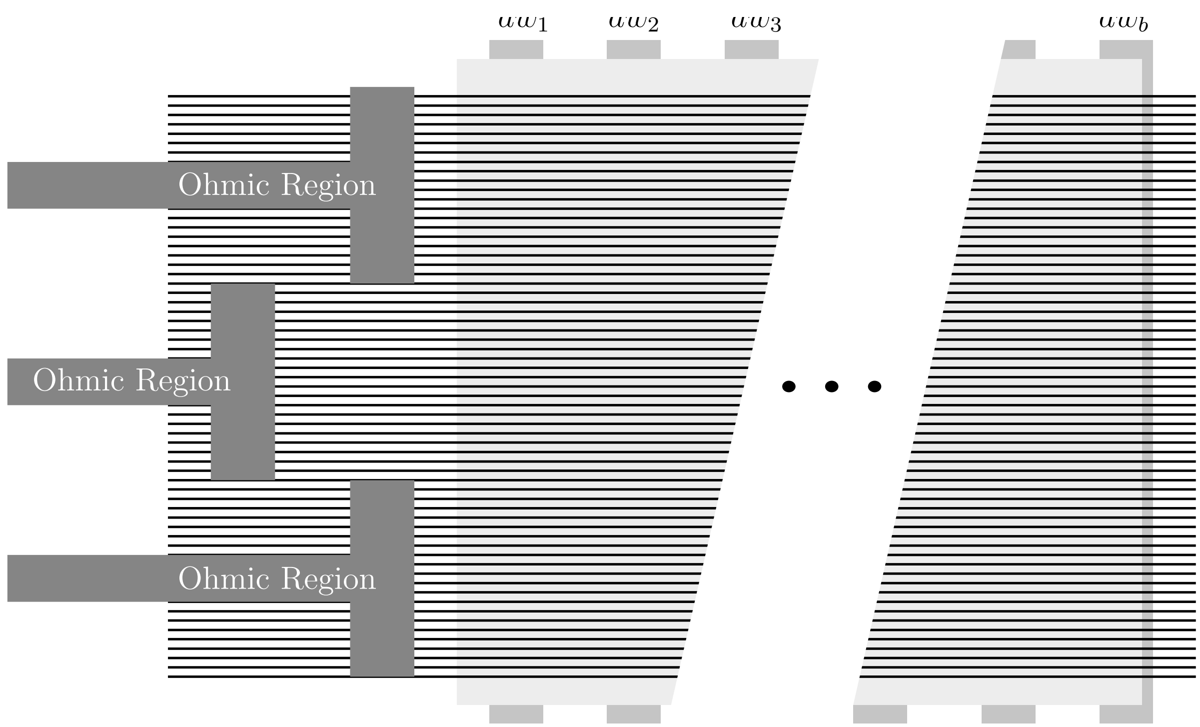
The Crossbar

- Programmable molecules (PMs) at NW crosspoints.
- Field-effect transistors (FETs) form at NW/MW junctions.
- NWs controlled by mesoscale wires (MWs).
- **Goal**: reliable control of NWs with few MWs.



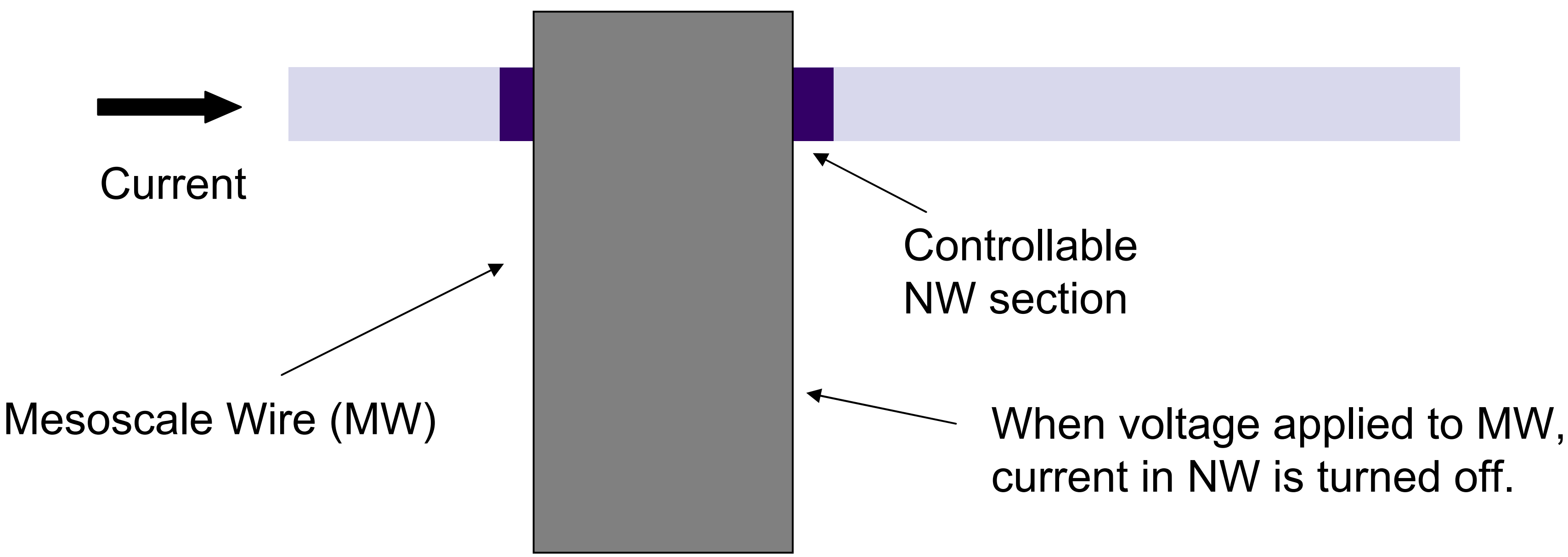
Multiple Simple Decoders

- They reduce the number of NW types needed.



Controlling NWs with MWs

- Grow NWs with controllable sections (FETs).
- Place MWs near these sections.



Types of NW Control

- Field effect control of NW resistance
  - Electric fields deplete regions of carriers
  - NWs can have lightly and heavily doped sections
  - Fields on NWs intensified by High-K dielectrics
- Binary versus modulated fields
  - In most decoders electric field is “on” or “off.”
  - Modulated fields used in an IBM device (IEDM’05)

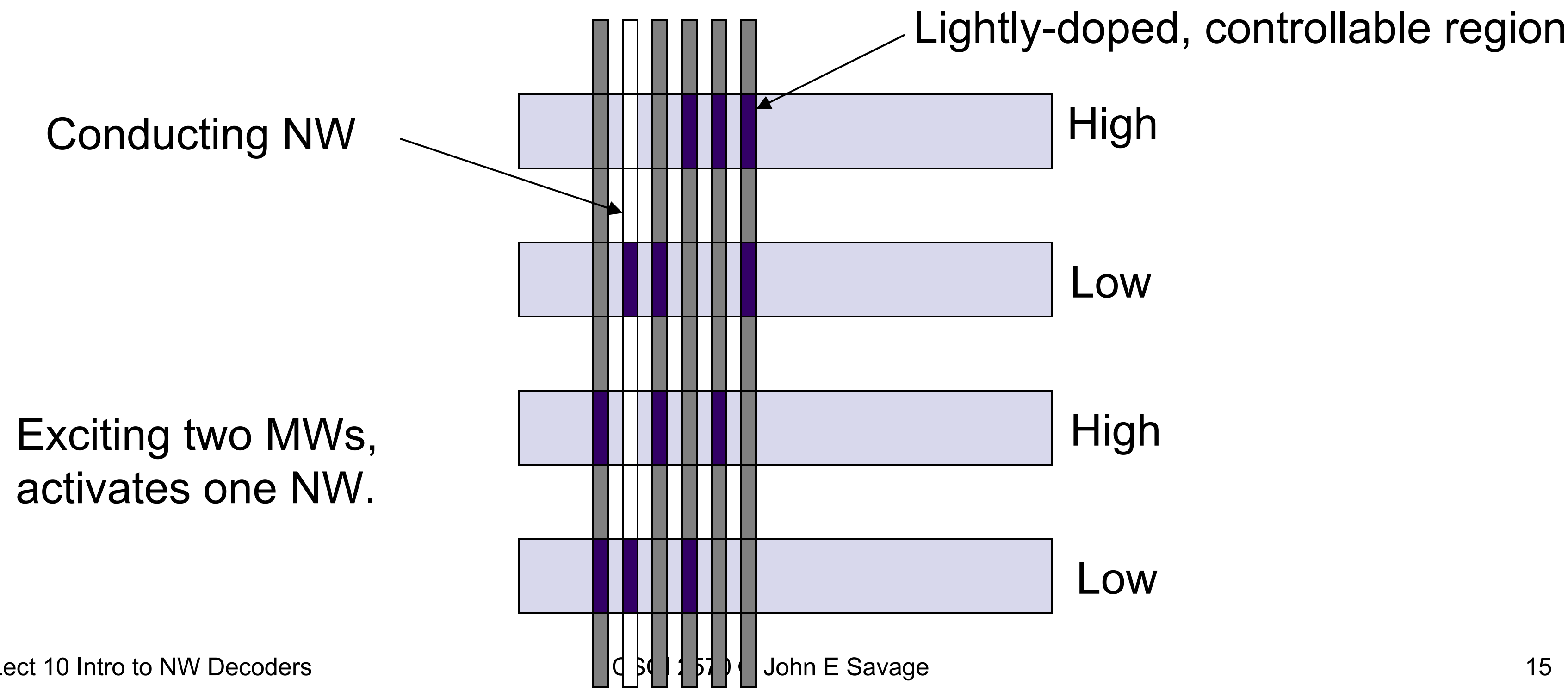
Uniform and Encoded Nanowires

- Two types of NW:
  - Uniform – deposited during assembly
  - Encoded – grown before assembly
- Uniform NWs deposited using nanostamping or nanolithographic methods
- Encoded NWs are grown in batches of one type, types are mixed and then deposited

Types of Simple Decoder

Decoding Mod-Doped NWs

- A meso-scale wire (MW) and lightly-doped NW region form field effect transistor (FET).

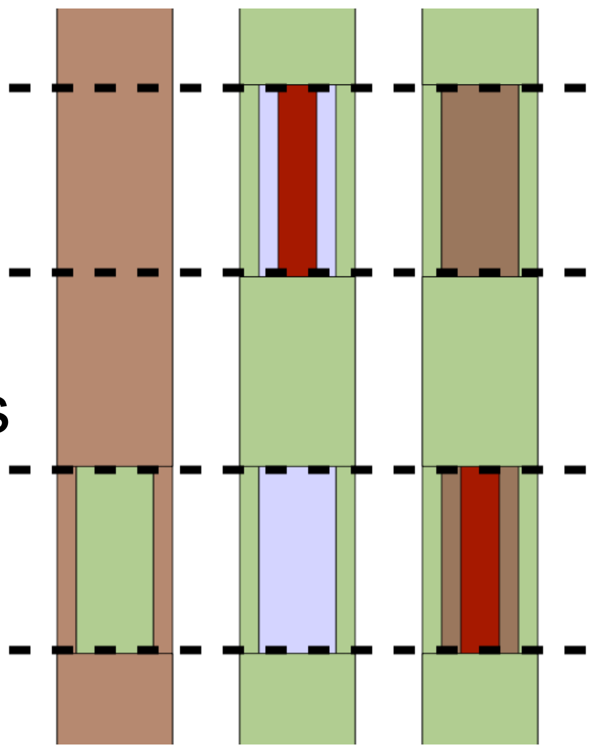


Issues with Mod-Doped NWs

- Because NWs are assembled fluidically, can't guarantee alignment of controllable regions with MWs.
- Need to mix NWs with different encoding patterns.
  - Can't guarantee that all patterns will appear.
  - Patterns may be repeated.

A Decoder for Core-Shell NWs

- NWs have *s* shells of *m* differentially etchable materials; materials in adjacent shells are different.
- They form $N = m(m-1)^{(s-1)}$ NW types.
- Under each MW etch the *s* materials forming a NW shell sequence.
- *N* NWs are controlled by *N* MWs.
- *12* codewords (and MWs) suffice to control 1,000 NWs for *w* = 10!

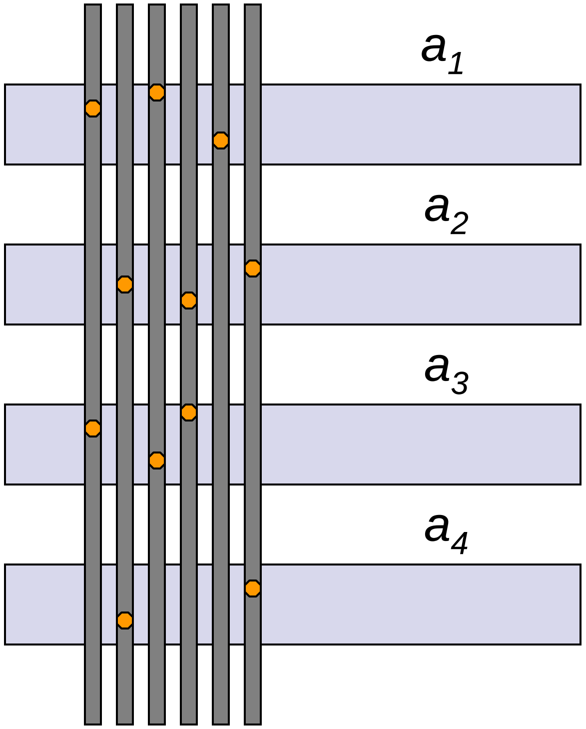


Issues with Core-Shell NWs

- Shells increase separation between NWs.
- Shells need to have uniform thickness.

Randomized Contact Decoder

- Gold particles are scattered at random so that with probability 0.5 there are particles between NW-MW pairs.
- Electric field on a MW turns a NW off if there is gold between them.
- How many MWs needed to control each NW?

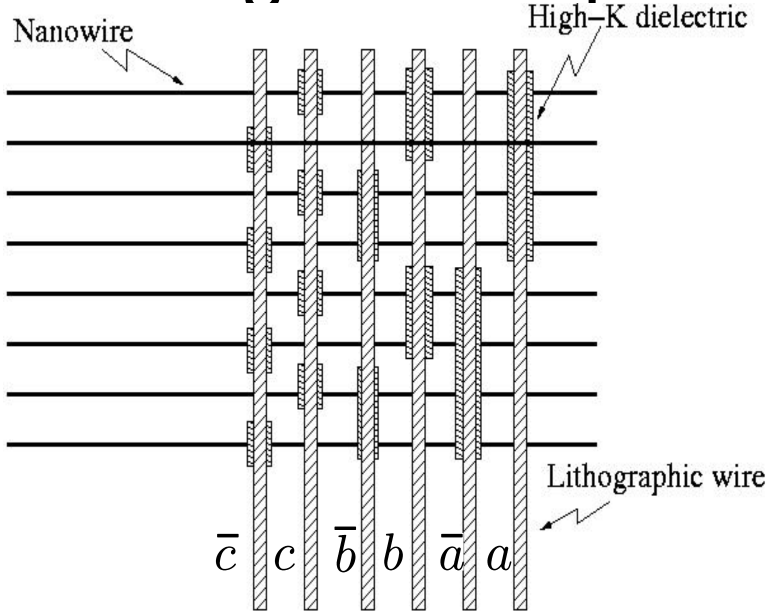


Issues with Randomized Contact Decoder

- Need a method to ensure uniformly random distribution of contacts between NWs and MWs.
- Need to model contacts providing limited control of NW by MW.

Deterministic Logarithmic Mask-Based Decoder

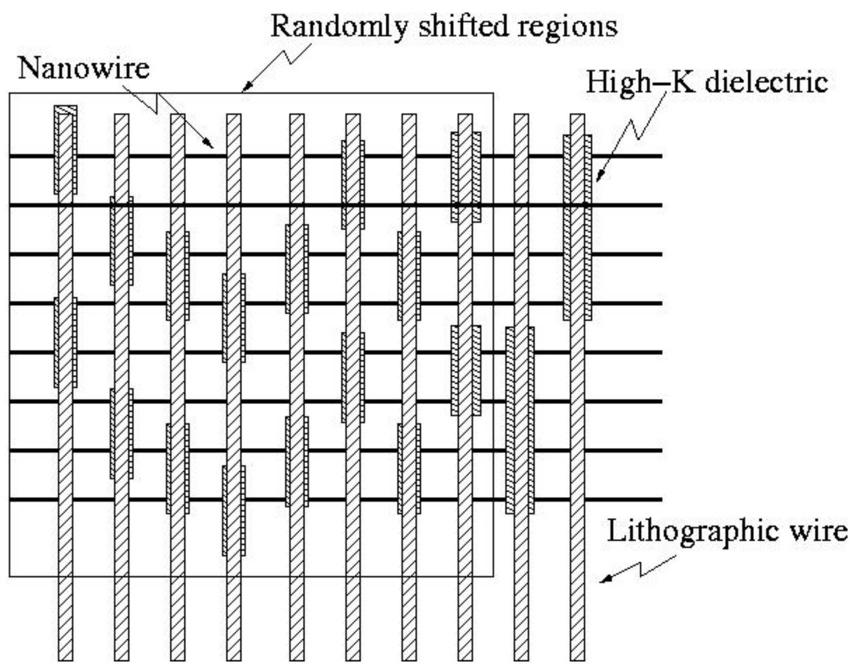
- High-K dielectric regions couple NWs & MWs



- Problem: can't make such small LRs or position them accurately

Randomized Mask-Based Decoder

- Randomly shift *M* copies of smallest litho regions to control all NWs with prob. > 1-ε



Issues with Mask-Based Decoder

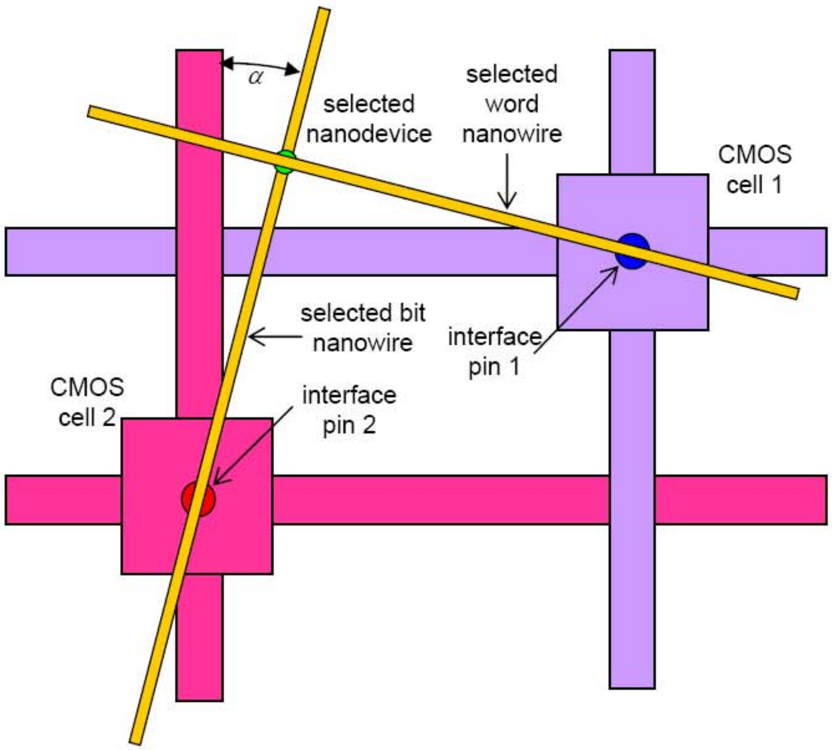
- Need to model displacement of masks.

- Should adjacent holes be put on the same or adjacent masks?

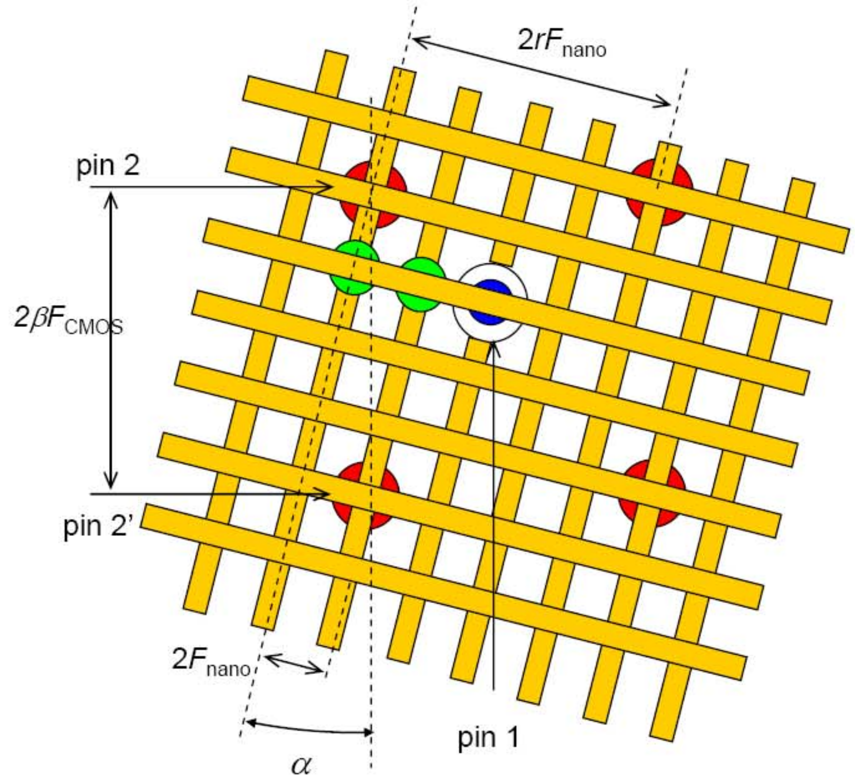
CMOL CONCEPT (II)

STONY BROOK
STATE UNIVERSITY OF NEW YORK

Most important: tilt $\alpha = \sin^{-1}(F_{nano}/\beta F_{CMOS})$



Nanodevice addressed via two CMOS cells



Every nanodevice may be addressed!

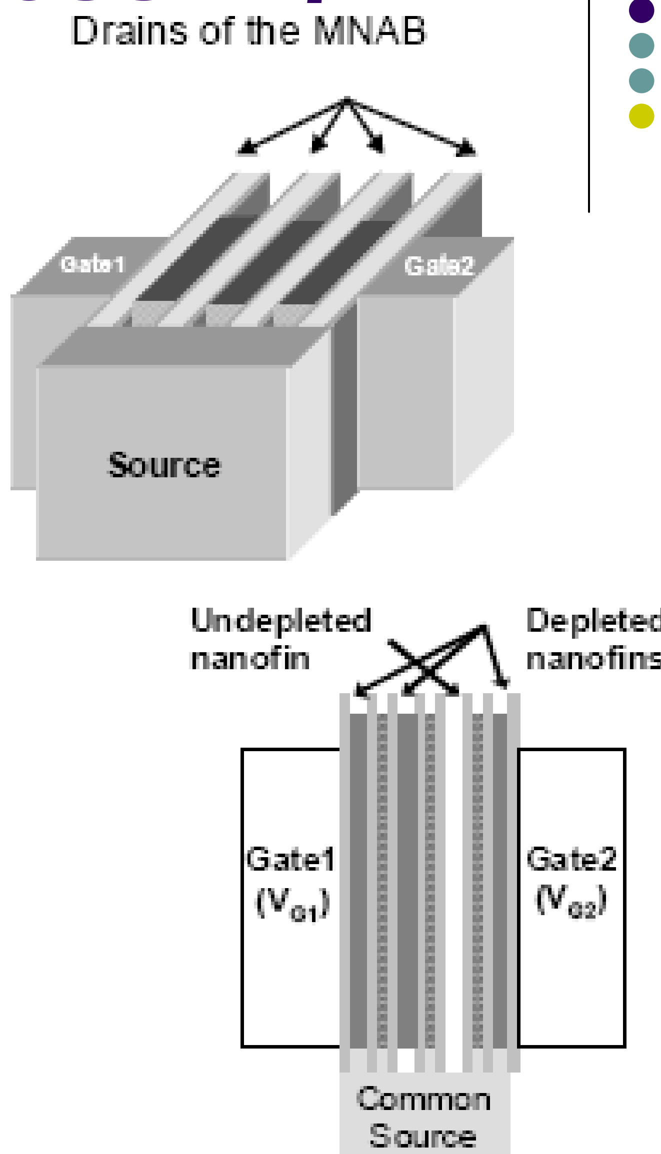
Portland, September 2005 13

Issues with CMOL

- What accuracy is needed in the angle between the coarse and fine grids?
- Can the nanoscale points of the correct length be formed on the coarse grid?

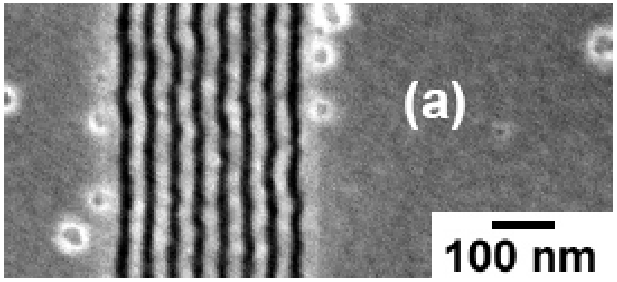
Micro to Nano Addressing Block (MNAB)

- IBM announced 4-fin device at 2005 IEDM.
- Claims:
  - Completely deterministic
  - Silicon based
  - No critical alignment
  - 100x current ratios between on & off NWs with 20nm NWs



Issues with MNAB

- Multiple voltage levels needed.
- Uncertainties in NW width and separation introduce uncertainties in voltages needed.

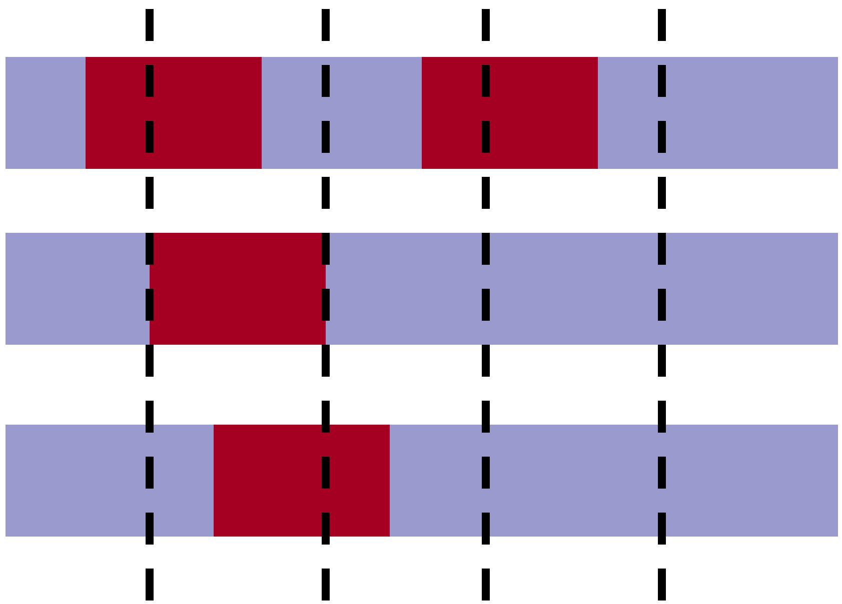


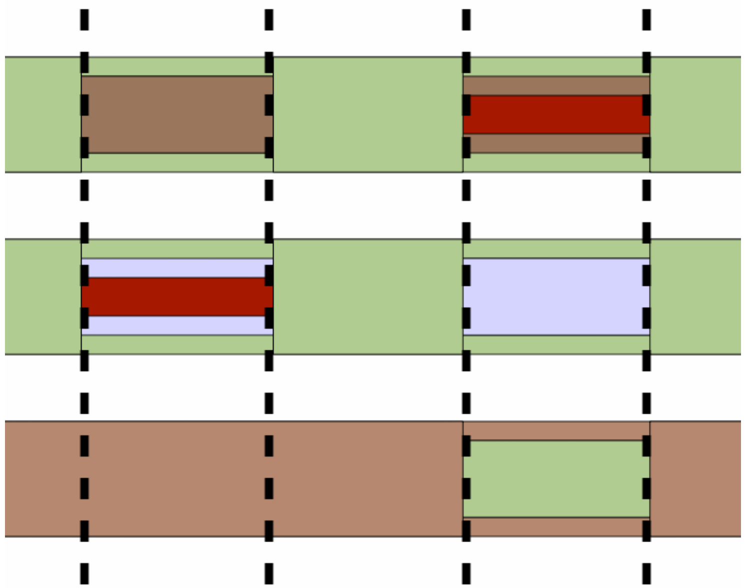
Models of Decoders

Alignment of Differentiated NWs

- Modulation-doped

Core-Shell





- Misaligned NWs

Aligned NWs

Ideal and Non-Ideal Decoder Models

- If NW is controlled (uncontrolled) by j^{th} MW,

  $c_j = 1$ ($c_j = 0$); M MWs.

- NW codeword $\boldsymbol{c} = (c_1, c_2, \ldots, c_M)$

- Ideal (non-ideal) resistive model
  - $c_j = 1$ if resistance = ∞ ($>r_{high}$) when j^{th} MW is on
  - $c_j = 0$ if resistance = 0 ($< r_{low}$) when j^{th} MW is off
  - $c_j = e$ (error) otherwise.

NW Addresses

Codewords Assigned to NWs by Stochastic Assembly

- Codeword for *i*th NW, n_i, is $\mathbf{c}^i = (c_1^i, c_2^i, \ldots, c_M^i)$

$$c_j^i = \begin{cases} 1 & j\text{th MW controls } i\text{th NW} \\ 0 & j\text{th MW doesn't control } i\text{th NW} \\ e & j\text{th MW control of } i\text{th NW ambiguous} \end{cases}$$

- If *j*th MW is “on” and $c_j^i = 1$, n_i is “off.”
- If *j*th MW is “off” and $c_j^i = 0$, n_i is “on.”
- If $c_j^i = e$, control of n_i is ambiguous.

Addressability of Nanowires

- NW n_i is **individually addressable** (**i.a.**) if there are "on" MWs causing n_i to be "on" &other NWs to be "off"

- $\boldsymbol{c}^2$ and $\boldsymbol{c}^4$ below are i.a.

  $\boldsymbol{c}^1 = (1,1,0,1,0)$

  $\boldsymbol{c}^2 = (1,0,1,0,0)$

  $\boldsymbol{c}^3 = (1,0,0,1,1)$

  $\boldsymbol{c}^4 = (1,0,0,1,0)$

- Codeword $\boldsymbol{c}$ is activated by address $\boldsymbol{a} = \overline{\boldsymbol{c}}$ (compl.)

NW Addressing Strategies

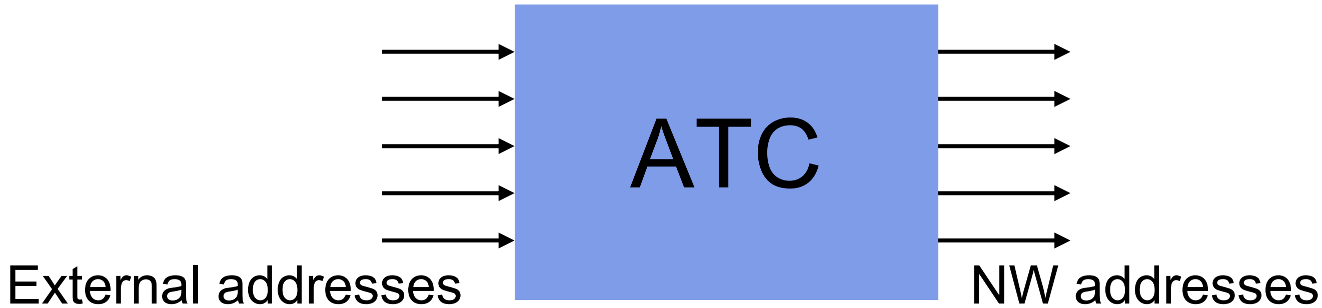
- All wires addressable in each contact group
  - Each NW in each group is individually addressable.
- Most wires addressable in each group
  - At least half the NWs in each group is individually addressable.
- All NW types present in each group
  - All *C* codewords are present in each group

More NW Addressing Strategies

- Each NW type occurs in *p* groups
  - All *C* codewords appear in *p* groups, *p* a fraction of *g*, the number of groups.
- All wires addressable in most groups
  - Introduce spare contact groups. In most groups, all NWs are different. Discard the others.
- Take What You Get
  - Use all individually addressable NWs in each contact group. Some will have more than others.

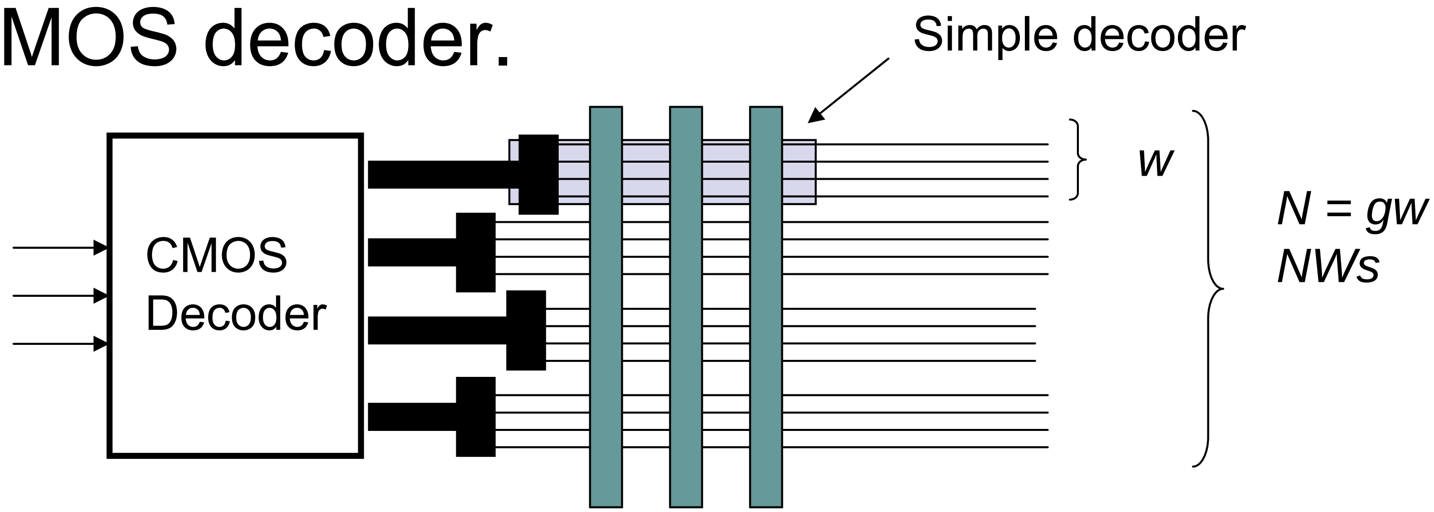
Address Translation

- Addresses assigned to NWs during assembly
  - Are unpredictable.
  - Must be discovered.
- External addresses are assigned to internal ones by **address translation circuit** (**ATC**).



Reducing the Area of the ATC

- The ATC has one word for each of the N_a addressable NWs.
- Area of ATC can be reduced by storing inputs to a CMOS decoder.



Crossbar Parameters

- g = number of contact groups.
- w = number of NWs per group.
- N = gw = number of NWs in each dimension.
- N_a = no. of i.a. NWs with probability ≥ $1-\varepsilon$.
- M = number of MWs.
- λ = ratio CMOS/nano feature size
- Crossbar stores N_a^2 values.
- $A = (M\lambda + N)^2 + 2A_{ATC}$ = area of Xbar + ATC

Comparison of NW Crossbars

- Crossbars are compared by the area they use for a given probability that N_a NWs are addressable.